

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-18 (canceled)

19. (Previously Presented) A state engine receiving multiple requests from a parallel processor for a shared state, the state engine comprising at least one state element means, said at least one state element means adapted to operate, atomically, on said shared state in response to a request made by said parallel processor.

20. (Previously Presented) A state engine as claimed in claim 19, wherein the operation performed by said at least one state element means is a single read-modify-write operation.

21. (Previously Presented) A state engine as claimed in claim 19, wherein said shared state comprises a single item of state.

22. (Previously Presented) A state engine as claimed in claim 19, wherein said shared state comprises multiple items of state.

23. (Previously Presented) A state engine as claimed in claim 19, wherein said state comprises a single storage location or a data structure in storage.

24. (Previously Presented) A state engine as claimed in claim 19, wherein the operation performed by said at least one state element means is carried out as a fixed or hardwired operation.

25. (Previously Presented) A state engine as claimed in claim 24, further comprising means to supply data to update said shared state.

26. (Previously Presented) A state engine as claimed in claim 24, further comprising means for sending a command and data to said shared state, whereby said operation is programmable.

27. (Currently Amended) A state engine as claimed in claim 19, further comprising a plurality of said state element means ~~organised~~ organized into state cell means, whereby operations performed on said shared state are pipelined.

28. (Previously Presented) A state engine as claimed in claim 27, further comprising a plurality of said state cell means, whereby to allow multiple requests to be handled concurrently.

29. (Previously Presented) A state engine as claimed in claim 28, further comprising input and output interconnect means providing access to and from said state cell means, a bus interface for said input and output interconnect means, said bus interface interfacing with a system bus and a control unit of a processing element for controlling accesses to said shared state.

30. (Previously Presented) A state engine as claimed in claim 27, wherein each said state element means comprises local memory, and each field of a data record is stored in a respective memory of a respective state element means.

31. (Previously Presented) A state engine as claimed in claim 19, wherein each said state element means comprises a local memory for said shared state, an arithmetic unit adapted to perform the operation on said state in said local memory, and command and control logic to control said operation.

32. (Previously Presented) A parallel processor including a state engine, said state engine receiving multiple requests from said parallel processor for a shared state,

the state engine comprising at least one state element means, said at least one state element means adapted to operate, atomically, on said shared state in response to a request made by said parallel processor.

33. (Previously Presented) A parallel processor as claimed in claim 32, wherein said parallel processor is an array processor.

34. (Previously Presented) A parallel processor as claimed in claim 33, wherein said array processor is a SIMD processor.

35. (Previously Presented) A computer system comprising a parallel processor, said parallel processor including a state engine, said state engine receiving multiple requests from said parallel processor for a shared state, the state engine comprising at least one state element means, said at least one state element means adapted to operate, atomically, on said shared state in response to a request made by said parallel processor.

36. (Previously Presented) A network processor comprising a parallel processor, said parallel processor including a state engine, said state engine receiving multiple requests from said parallel processor for a shared state, the state engine comprising at least one state element means, said at least one state element means

adapted to operate, atomically, on said shared state in response to a request made by said parallel processor.

37. (Previously Presented) A parallel processor as claimed in claim 32, implemented on a single silicon chip.

38. (New) A state engine receiving multiple requests from a parallel processor for a shared state, the state engine comprising:

means for operating, atomically, on said shared state in response to a request made by said parallel processor; and

means to supply data to update said shared state.